Lec. 4 control instruction and op-code

1. **Control instructions**
   a. **NOP**
      - ✓ No operation
      - ✓ No operation is performed.
      - ✓ The instruction is fetched and decoded but no operation is executed.
      - ✓ Example: NOP

   b. **HLT**
      - ✓ Halt
      - ✓ The CPU finishes executing the current instruction and halts any further execution.
      - ✓ An interrupt or reset is necessary to exit from the halt state.

2. **Op-code**:

The complete set of instructions supported by a microprocessor is called its Instruction Set. Intel's 8085 has 246 instructions. A binary value denotes each instruction of the 8085. These 8-bit binary values are called Op-Codes or Instruction Bytes.

The op-code is the first part of an instruction that specifies the operation that is to be performed. Whereas, the operand is the second (or third) part of the instruction on which the operation is performed. You'll understand this more clearly as we progress through the instruction set.

HEX	MNEMONIC	
CE	ACI	8 bit
8F	ADC	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
87	ADD	A
80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
C6	ADI	8 bit
A7	ANA	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
E6	ANI	8-Bit
CD	CALL	16-bit
DC	CC	16-bit
FC	CM	16-bit
2F	CMA	
3F	CMC	
BF	CMP	A
B8	CMP	B

HEX	MNEMONIC	
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
D4	CNC	16-bit
C4	CNZ	16-bit
F4	CP	16-bit
EC	CPE	16-bit
FE	CPI	8-bit
E4	CPO	16-bit
CC	CZ	16-bit
27	DAA	
9	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP
3D	DCR	A
5	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP
F3	DI	
FB	EI	
76	HLT	
DB	IN	8-bit

HEX	MNEMONIC	
3C	INR	A
4	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3	INX	B
13	INX	D
23	INX	H
33	INX	SP
DA	JC	16-bit
FA	JM	16-bit
C3	JMP	16-bit
C2	JNZ	16-bit
F2	JP	16-bit
EA	JPE	16-bit
E2	JPO	16-bit
CA	JZ	16-bit
3A	LDA	16-bit
0A	LDAX	B
1A	LDAX	D
2A	LHLD	16-bit
01	LXI	B,16-bit
11	LXI	D,16-bit
21	LXI	H,16-bit
31	LXI	SP,16-bit
7F	MOV	A,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H

HEX	MNEMONIC	
7D	MOV	A,L
7E	MOV	A,M
47	MOV	B,A
40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
4F	MOV	C,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
57	MOV	D,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MOV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
5F	MOV	E,A
58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M

HEX	MNEMONIC	
67	MOV	H,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
6F	MOV	L,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
77	MOV	M,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L
3E	MVI	A,8-bit
06	MVI	B,8-bit
0E	MVI	C,8-bit
16	MVI	D,8-bit
1E	MVI	E,8-bit
26	MVI	H,8-bit
2E	MVI	L,8-bit
36	MVI	M,8-bit
0	NOP	
B7	ORA	A
B0	ORA	B

HEX	MNEMONIC	
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
F6	ORI	8-bit
D3	OUT	8-bit
E9	PCHL	
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW
C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
17	RAL	
1F	RAR	
D8	RPE	
C9	RET	
20	RIM	
7	RLC	
F8	RM	
D0	RNC	
C0	RNZ	
F0	RP	
E8	RPE	
E0	RPO	
0F	RRC	
C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3

HEX	MNEMONIC	
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7
C8	RZ	
9F	SBB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
DE	SBI	8-bit
22	SHLD	16-bit
30	SIM	
F9	SPHL	
32	STA	16-bit
2	STAX	B
12	STAX	D
37	STC	
97	SUB	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
D6	SUI	8-bit
EB	XCHG	
AF	XRA	A
A8	XRA	B
A9	XRA	C

HEX	MNEMONIC	
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
EE	XRI	8-bit
E3	XTHL	

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Example: write this program in machine language (op-code)?

```
MVI A 00h
LXI H 1000h
MVI C 0Ch

START: ADD M
INX H
DCR C
JNZ START

INX H

MOV M A
```

Hex Code Grid

Address	Data
8000	3E
8001	00
8002	21
8003	00
8004	10
8005	0E
8006	0C
8007	86
8008	23
8009	0D
800A	C2
800B	07
800C	80
800D	23
800E	77

Lec.5 8085 Instruction Cycle and timing diagram

1. **Microprocessor's instruction**:
   a. An instruction consist of
      - ✓ A command called operation code (op-code)
      - ✓ Operand (either data, address, or register)

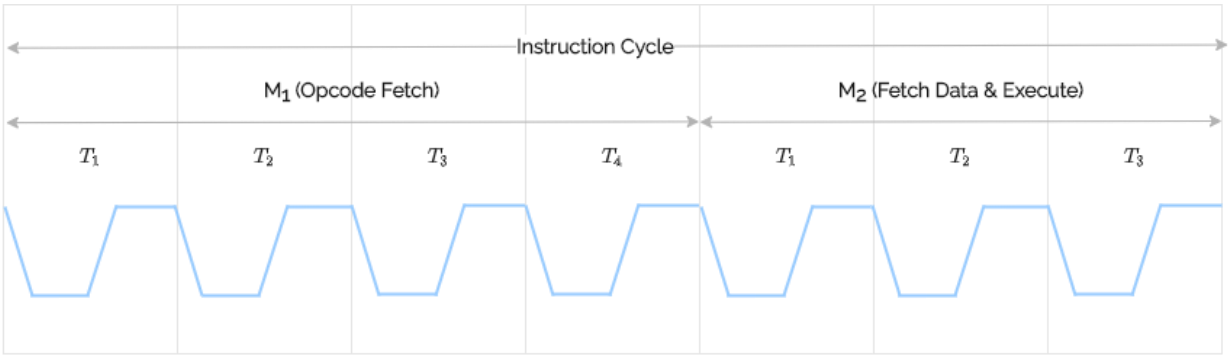
   b. Execution an instruction requires
      - ✓ Fetching
      - ✓ Decoding
      - ✓ Execution

2. **Instruction execution length**: the time required to execute an instruction is measured by :
   - ✓ **T-states:** equals the time of one clock period = $\frac{1}{f}$, f= microprocessor's operating frequency.
   - ✓ **Machine cycle:** the time required to finish one operation (fetching or reading/writing to/from memory/IO)
   - ✓ **Instruction cycle:** the time required to fully execute a complete instruction.

3. **Timing diagram**

   Consist of :
   - ✓ Time cycle
   - ✓ Higher order address bus
   - ✓ Lower order address/data bus
   - ✓ ALE
   - ✓ IO/$\overrightarrow{M}$ with S0 and S1
   - ✓ $\overline{RD}$
   - ✓ $\overline{WR}$

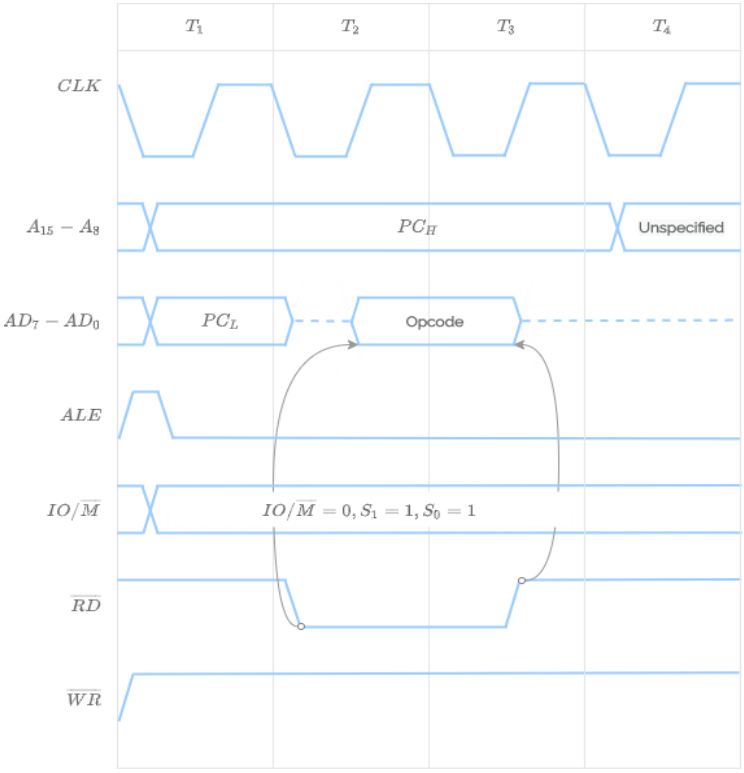
A typical instruction cycle and the machine cycles within it is shown in the figure.



Op-code Fetch Machine Cycle

Every instruction's first machine cycle is an op-code fetch machine cycle, during which the 8085 microprocessor determines the type of instruction to be executed. The following figures show the timing diagram for the op-code fetch machine cycle.

EX: 2000 MOV A C



The number of states in the op-code fetch machine cycle may vary from 4T states.

The following is a detailed step-by-step explanation of the op-code fetch cycle.

1. **State T1**
   - Places the contents of PC on the address bus.
   - The higher order bits (PCH) is placed on the A15-A8 lines.
   - The lower order bits (PCL) is placed on the AD7-AD0 lines.
   - ALE signal goes high in the beginning to indicate that AD7-AD0 contains lower address bits.
   - The status signals IO/$\overline{M}$ specifies whether it is a memory or I/O operation.
   - The S1 status signal specifies whether it is read/write operation.
   - In op-code fetch machine cycles status signals are: IO/$\overline{M}$= 0, S1=1, S0 = 1.

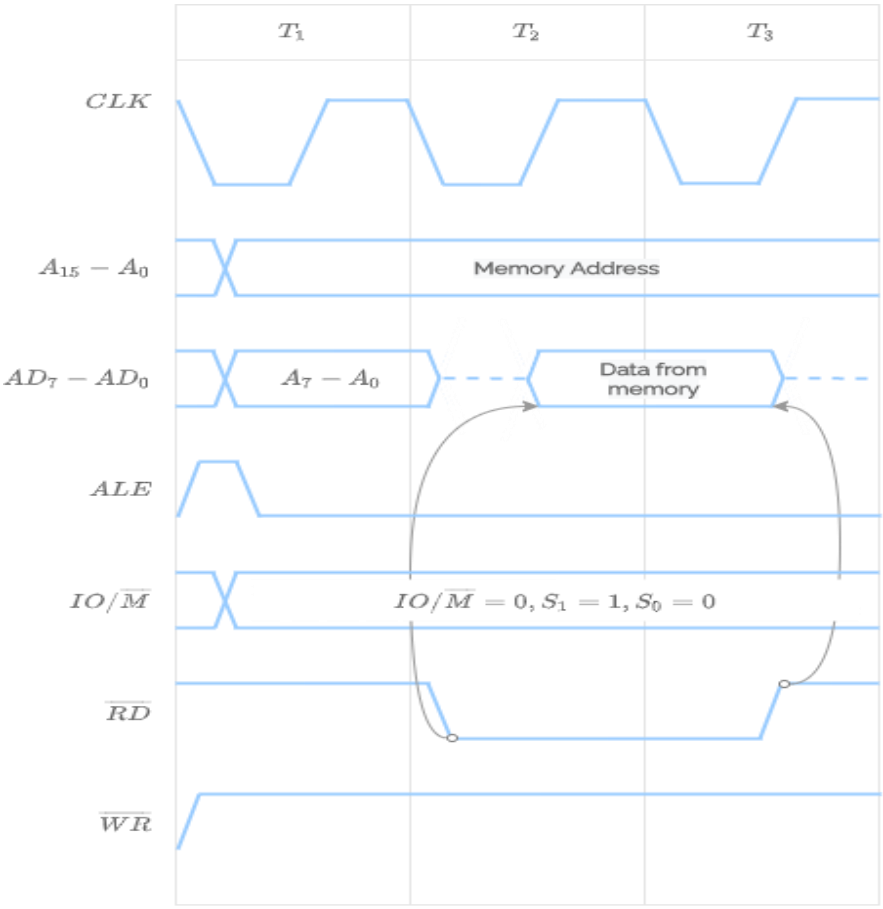
2. **State T2**
   - The lower order address disappears from the AD7-AD0 lines.
   - The $\overline{RD}$ signal is set to 0 to enable the addressed memory location.
   - The contents of addressed memory location is placed on the data bus (AD7-AD0).

3. **State T3**
   - The op-code is loaded into the instruction register from the data bus.
   - The $\overline{RD}$ is raised to 1 which disables the memory device.

4. **State T4**
   - Decodes the op-code.

Memory Read Machine Cycle

During the memory read machine cycle, the contents of a memory location are read. This machine cycle is made up of three T states. The first three T states are almost the same as the first three T states of the Op-code Fetch Machine Cycle. The following figures show the timing diagram for the memory read machine cycle.



The following is a detailed step-by-step explanation of the memory read machine cycle.

1. State T1

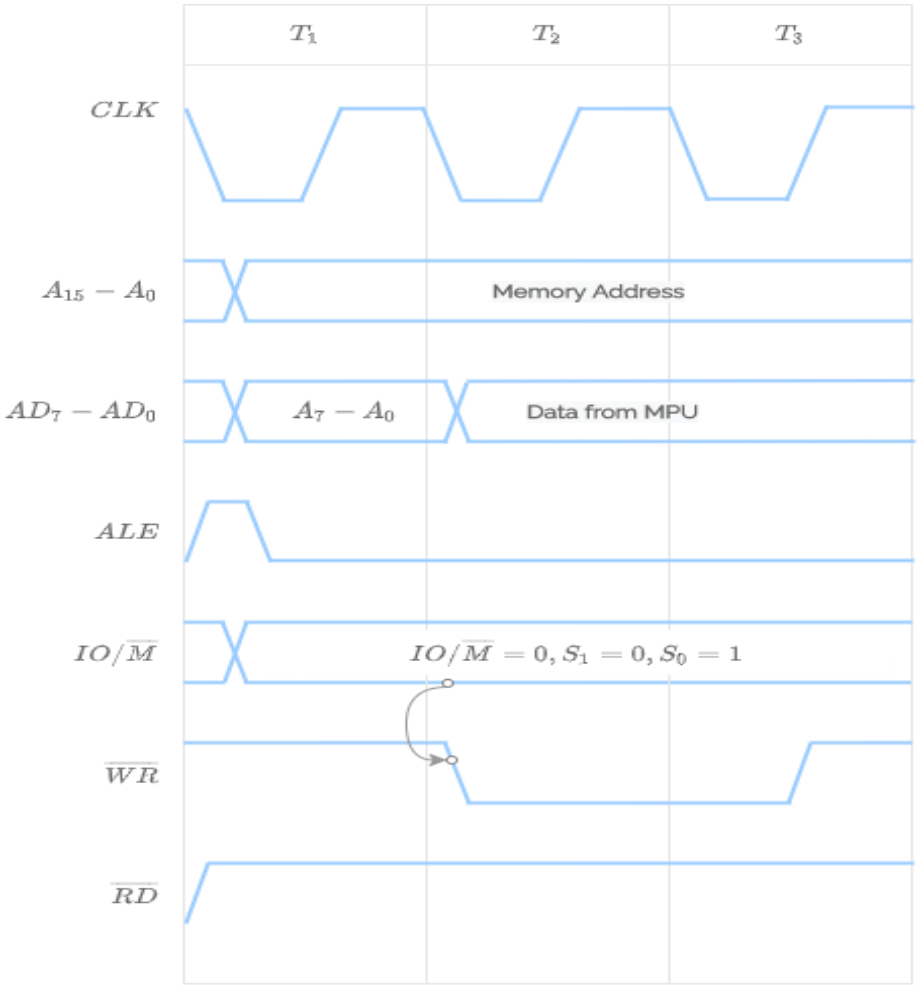
- Higher address bits have been loaded into A8-A15.
- Lower address bits have been loaded into AD0-AD7.
- In the beginning, the ALE signal is high, indicating that AD0-AD7 includes lower address bits.
- IO/$\overline{M}$goes low since it is a memory operation.
- S1 and S0 become 1 and 0, signifying a Memory Read Machine Cycle.
- By the end of the first T state, ALE goes low.

2. State T2 and T3

- $\overline{RD}$ goes low, indicating that the read process takes place.
- Data is read from memory and placed onto the data bus AD0-AD7.
- The data is loaded into the data bus at the start of the T2 state and remains in place until the end of the T3 state.
- $\overline{RD}$ gets high at the end of the T3 state, signifying the end of the read operation.

Memory Write Machine Cycle

Contents are written to a memory location/stack during a memory write machine cycle. This machine cycle is made up of three T states. The following figures show the timing diagram for the memory write machine cycle.



The following is a detailed step-by-step explanation of the memory write machine cycle.

1. **State T1**
   - Higher address bits have been loaded into A8-A15.
   - Lower address bits have been loaded into AD0-AD7.
   - In the beginning, the ALE signal is high, indicating that AD0-AD7 includes lower address bits.
   - IO/$\overline{M}$goes low since it is a memory operation.
   - S_1 and S_0 become 0 and 1, signifying a Memory Write Machine Cycle.
   - By the end of the first T state, ALE goes low.

2. **State T2 and T3**
   - $\overline{WR}$ goes low, indicating that the write process has begun.
   - Data to be written is loaded onto the data bus at the start of the T2 state and remains on the data bus until the end of the T3 state.
   - $\overline{WR}$ goes high at the end of the T3 state, signifying the end of the write operation.

Examples1: The DCR instruction in MP 8085 has has 1 machine cycle, i.e. opcode fetch cycle. But the DCR M instruction has 3 machine cycles. What are those three machine cycles?

Sol. The 3 machine cycles are:

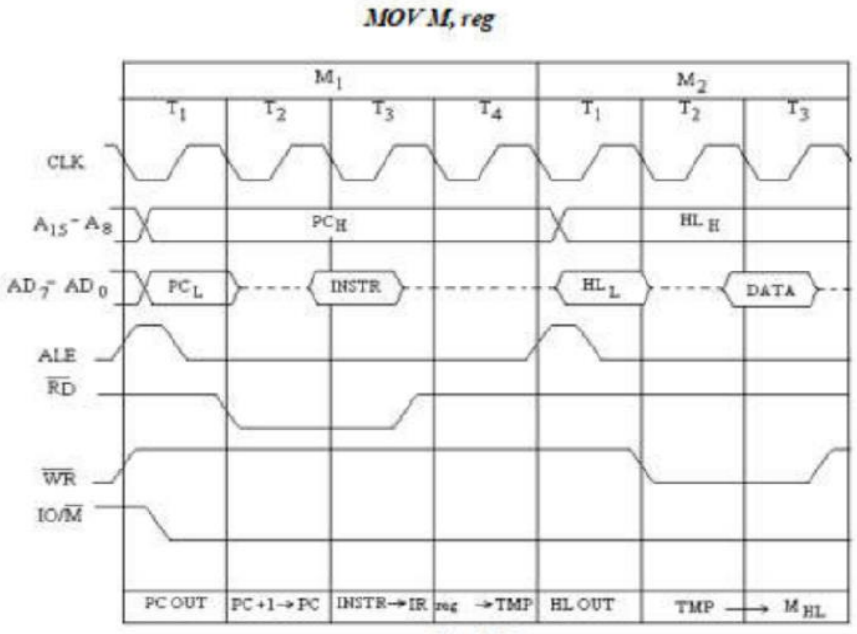
1. Op-code Fetch Cycle
2. Memory Read Cycle
3. Memory Write Cycle

Examples2:

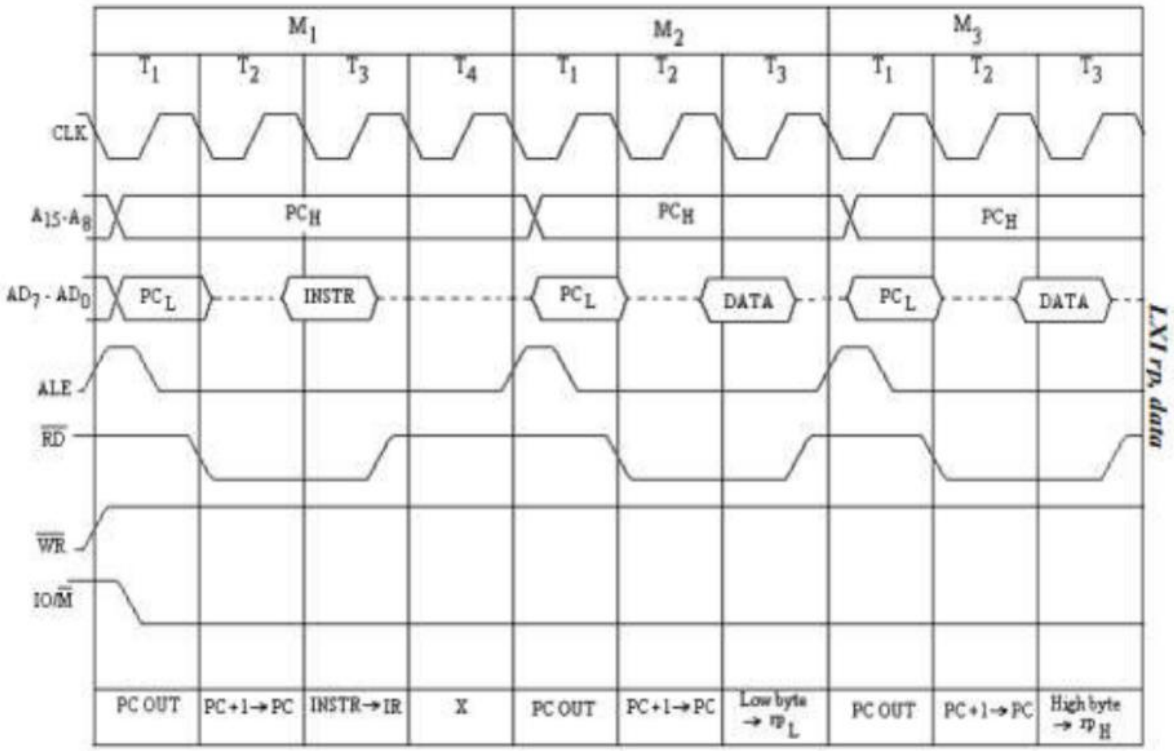
Instruction	No. of bytes	No. of cycles	No. of T-state
MOV A C	1	1	4
ADD R	1	1	4
ACI data	2	2	7
MVI 35h	2	2	7
LXI H,2000h	3	3	10
DCR M	1	3	10
LDA 2000	3	4	13

Examples: draw the timing diagram for these instructions:

1. MOV M,R



2. LXI Rp, data



3. HLT