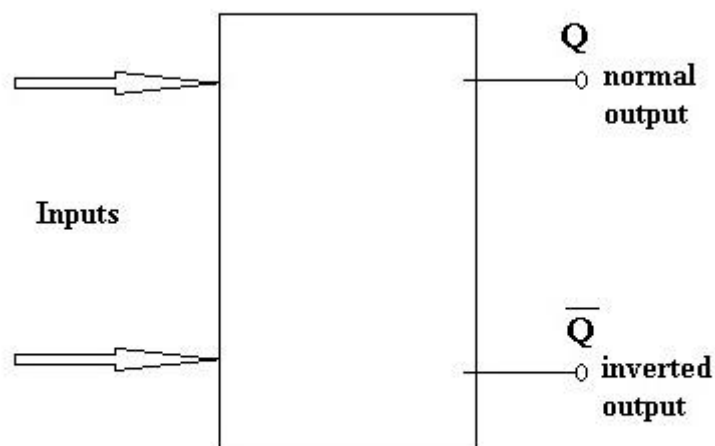


Flip-Flops :-

Flip-flop(FF) is the most important memory element which is made up of an assembly of logic gates. Even though a logic gate, by itself, has no storage capability, several can be connected together in ways that permit information to be stored.

The general form of FF's is shown in the figure below

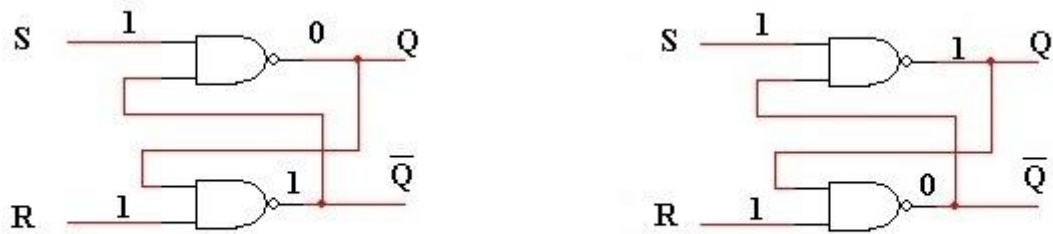


If: $Q=1$, $\bar{Q}=0$ called High or 1 state, also called Set state

If: $Q=0$, $\bar{Q}=1$ called Low or 0 state, also called Reset state

NAND Gate Latch :-

The most basic FF circuit can be constructed from either two NAND gated or two NOR gates. The NAND gate version, called a NAND gate latch or simply a latch, is shown in the figure below.

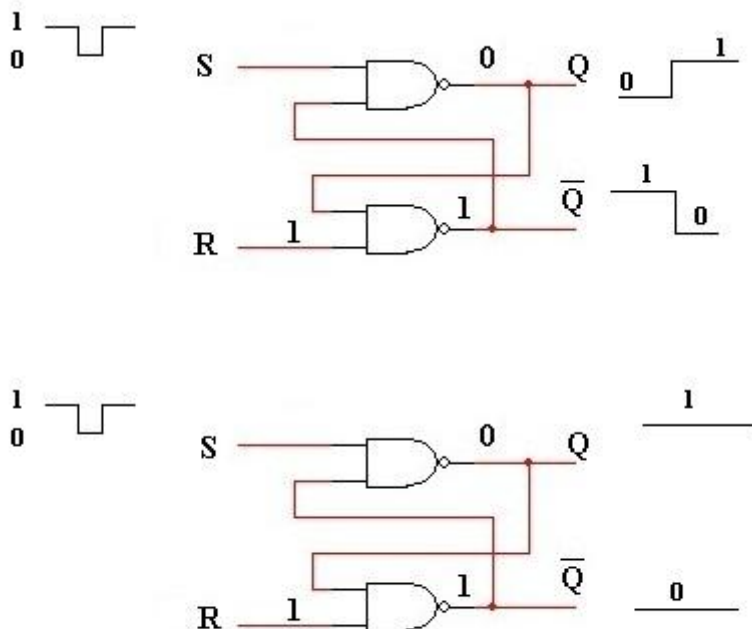


$S = R = 1$ (resting state)

The above figure shows the two possibility for resting case (the S and R are normally resting in High state).

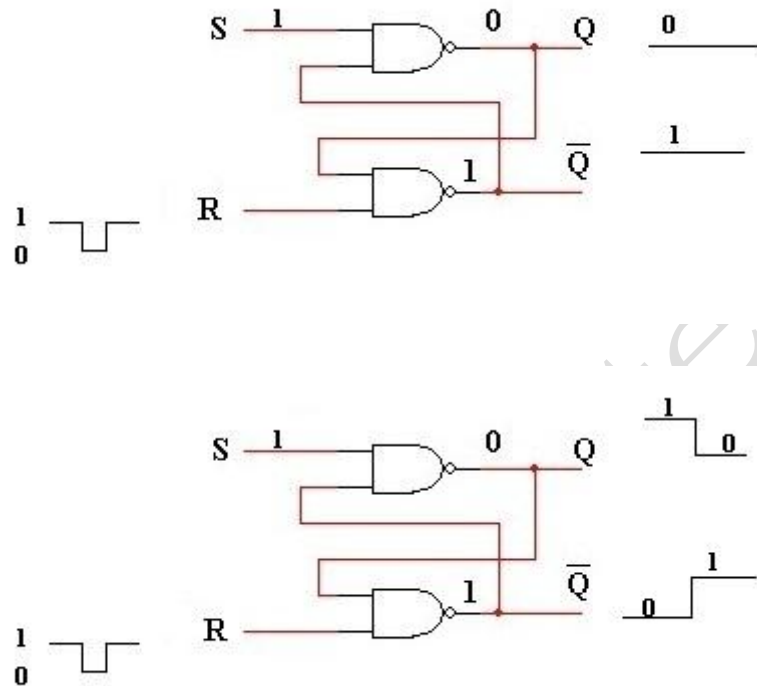
Setting the latch (FF) :-

It is performed when the input S is momentarily pulsed Low while R is kept High as shown in the figure below.



Clearing the latch (FF) :-

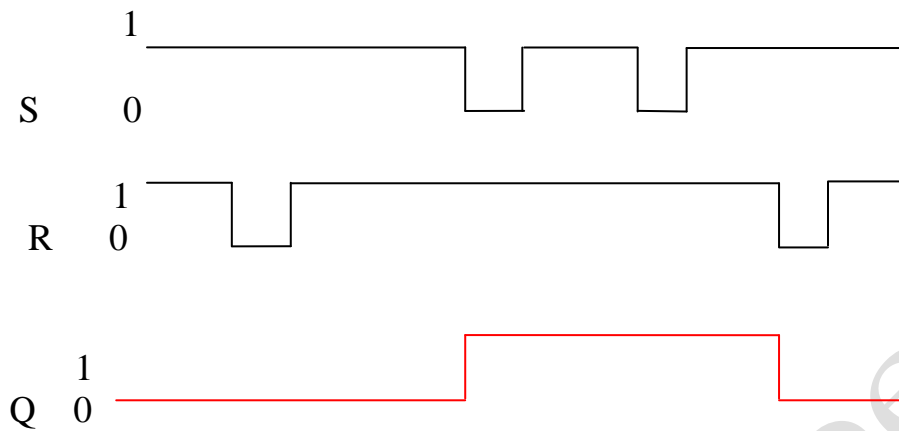
It is performed when R input is pulsed Low while S is kept High. The following figure shows the two possibilities.



The operation described above can be conveniently in a truth table :

S	R	Q	\bar{Q}
0	0	Invalid (produces $Q = \bar{Q} = 1$)	
0	1	1	0
1	0	0	1
1	1	No change	

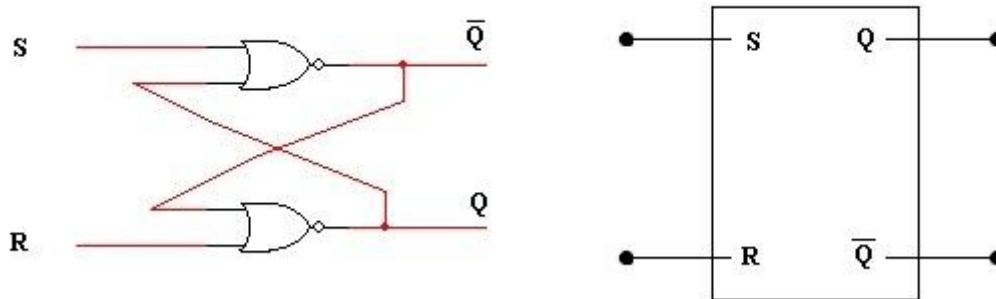
The waveforms shown below are applied to the NAND latch. Assume that initially $Q=0$, determine the Q waveform.



H.W :- repeat the example for Q initially equal 1 .

NOR Gate Latch (FF) :-

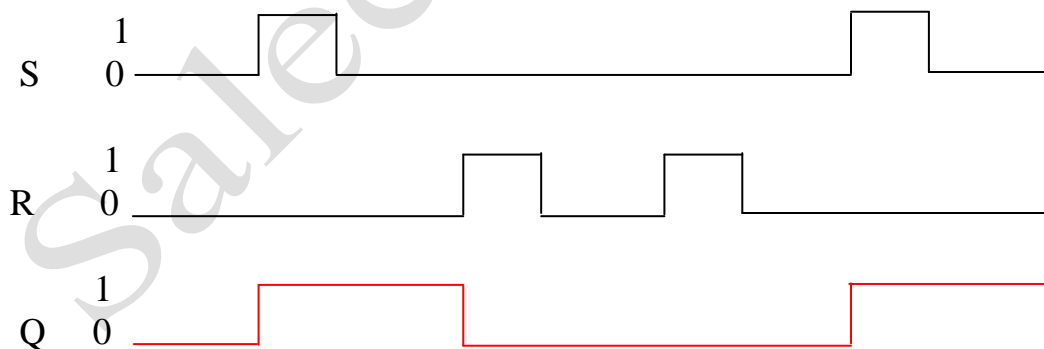
The arrangement of this latch (FF) is shown below :



S	R	Q
0	0	No change
0	1	0
1	0	1
1	1	invalid

Example :

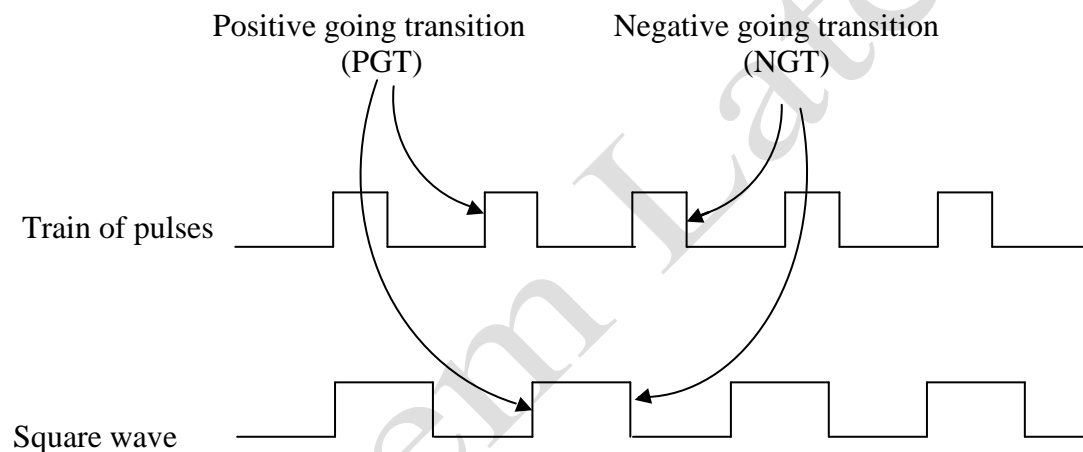
Assume that $Q=0$ initially, determine the Q waveform for the NOR latch with inputs shown below.



Clock signal :-

Digital systems can operate either asynchronously or synchronously. In asynchronous systems, the outputs of logic circuits can change state any time one or more of inputs change.

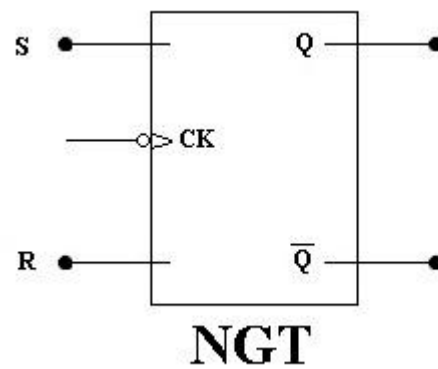
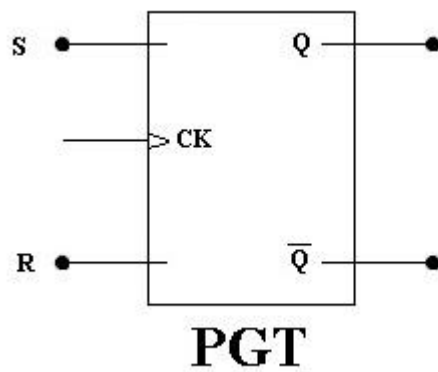
In synchronous systems, the exact times at which any output can change states is determined by a signal commonly called the clock. This clock signal is generally a rectangular pulse train or square wave as shown below.



Clocked Flip-Flops :-

There are several types of clocked FFs that are used in a wide range of applications. The principle ideas that are common to all of them are:

- 1) Clocked FFs have a clock input that is labeled CLK, CK, or CP.
- 2) The inputs will have no effect on Q until the clock transition occurs.
- 3) The active clock transition is either PGT or NGT as shown in the figure below.



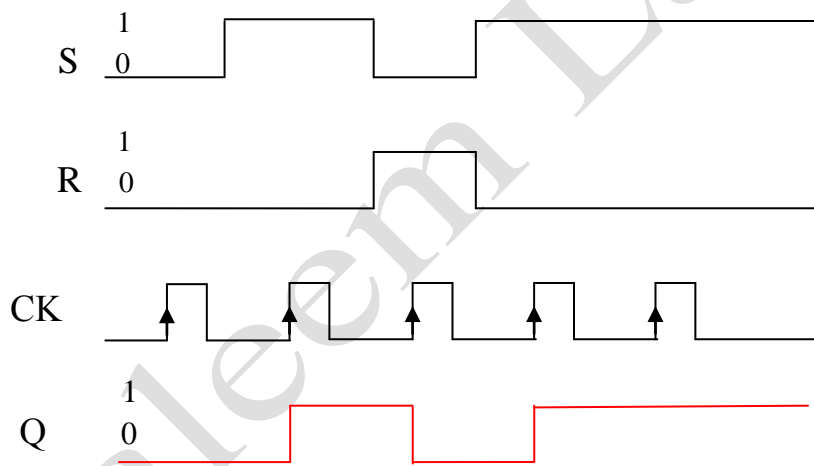
Clocked S-R FF :-

The truth table of clocked S-R FF with PGT clock is :-

S	R	CK	Q
0	0	↑	No change
1	0	↑	1
0	1	↑	0
1	1	↑	invalid

Example :-

Determine the output waveform for the following input waveforms to the clocked FF. The output initially zero (Q=0)



H.W:-

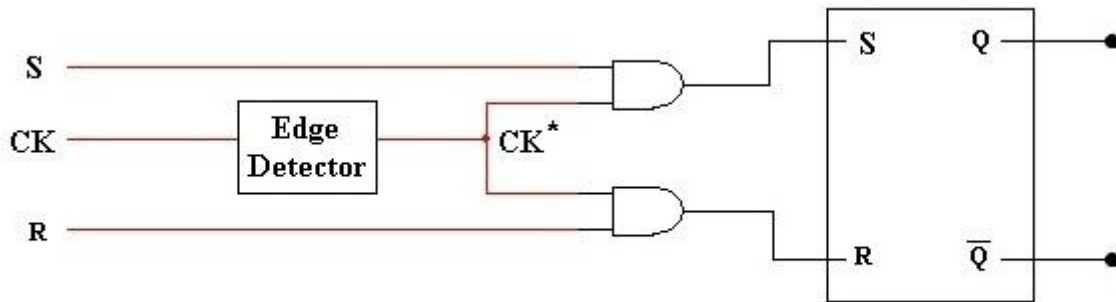
Determine the output waveform for the previous clocked FF with NGT.

Hint:- The truth table of clocked S-R FF with NGT is :

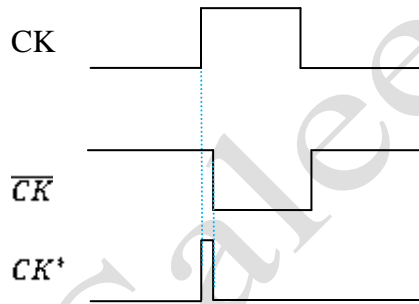
S	R	CK	Q
0	0	↓	No change
1	0	↓	1
0	1	↓	0
1	1	↓	invalid

Internal circuitry of clocked S-R FF :-

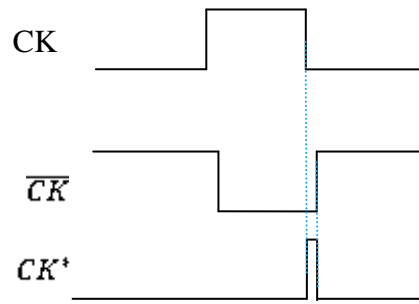
The figure below shows the internal circuit of clocked S-C FF.



The figure below shows the circuit edge detector.



(PGT)

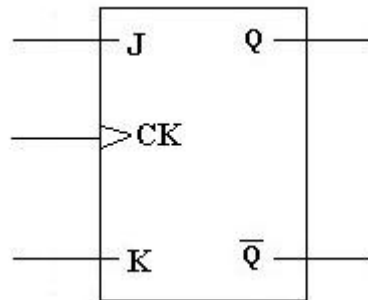


(NGT)

Clocked J-K FF :-

The JK flip-flop augments the behavior of the SR flip-flop (J=Set, K=Reset) by interpreting the $S = R = 1$ condition as a "flip" or toggle command. Specifically, the combination $J = 1, K = 0$ is a command to set the flip-flop; the combination $J = 0, K = 1$ is a command to reset the flip-flop; and the combination $J = K = 1$ is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value.

The figure below shows the symbol of J-K FF :-

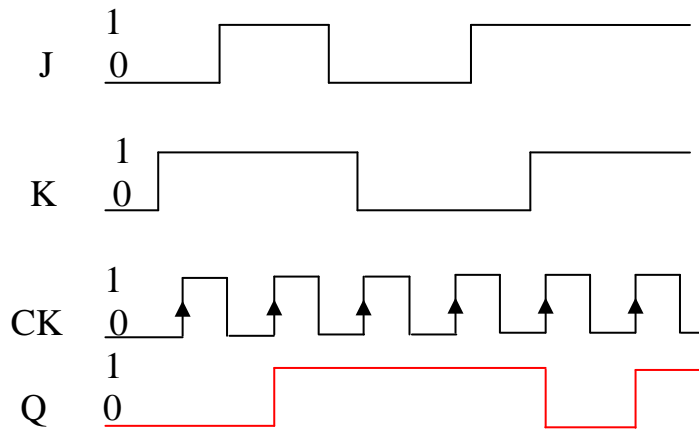


A circuit symbol for a Positive edge triggered JK flip-flop, where \triangleright is the clock input, J and K are data inputs, Q is the stored data output, and Q' is the inverse of Q

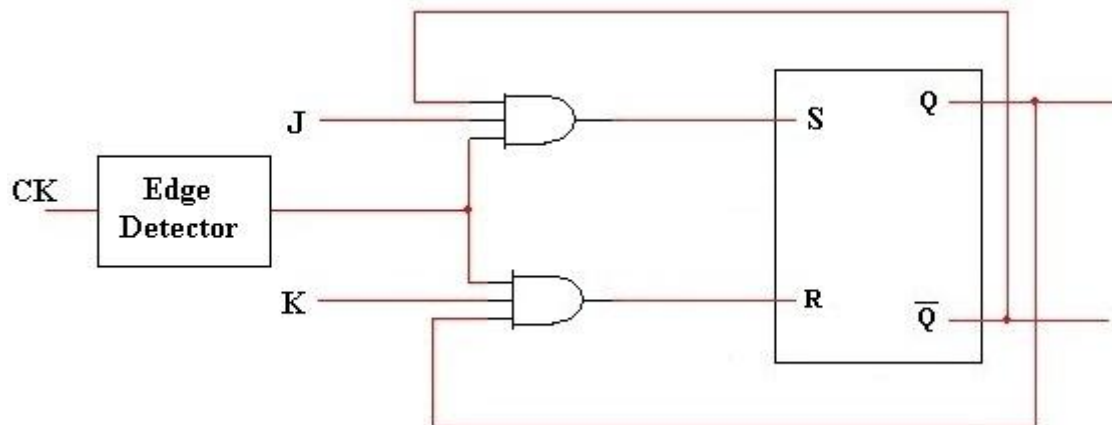
The characteristic equation of the JK flip-flop is:

$$Q_{next} = J\bar{Q} + \bar{K}Q$$

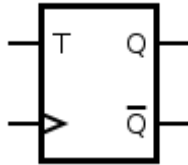
J	K	CK	Q
0	0	↑	Q_0 (No change)
0	1	↑	0
1	0	↑	1
1	1	↑	\bar{Q}_0 (Toggle)



Internal circuit of clocked J-K FF :-



T-type FF :-



A circuit symbol for a T-type flip-flop, where \triangleright is the clock input, T is the toggle input and Q is the stored data output. If the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip-flop holds the previous value. This behavior is described by the characteristic equation :

$$Q_{next} = T \oplus Q = T\bar{Q} + \bar{T}Q$$

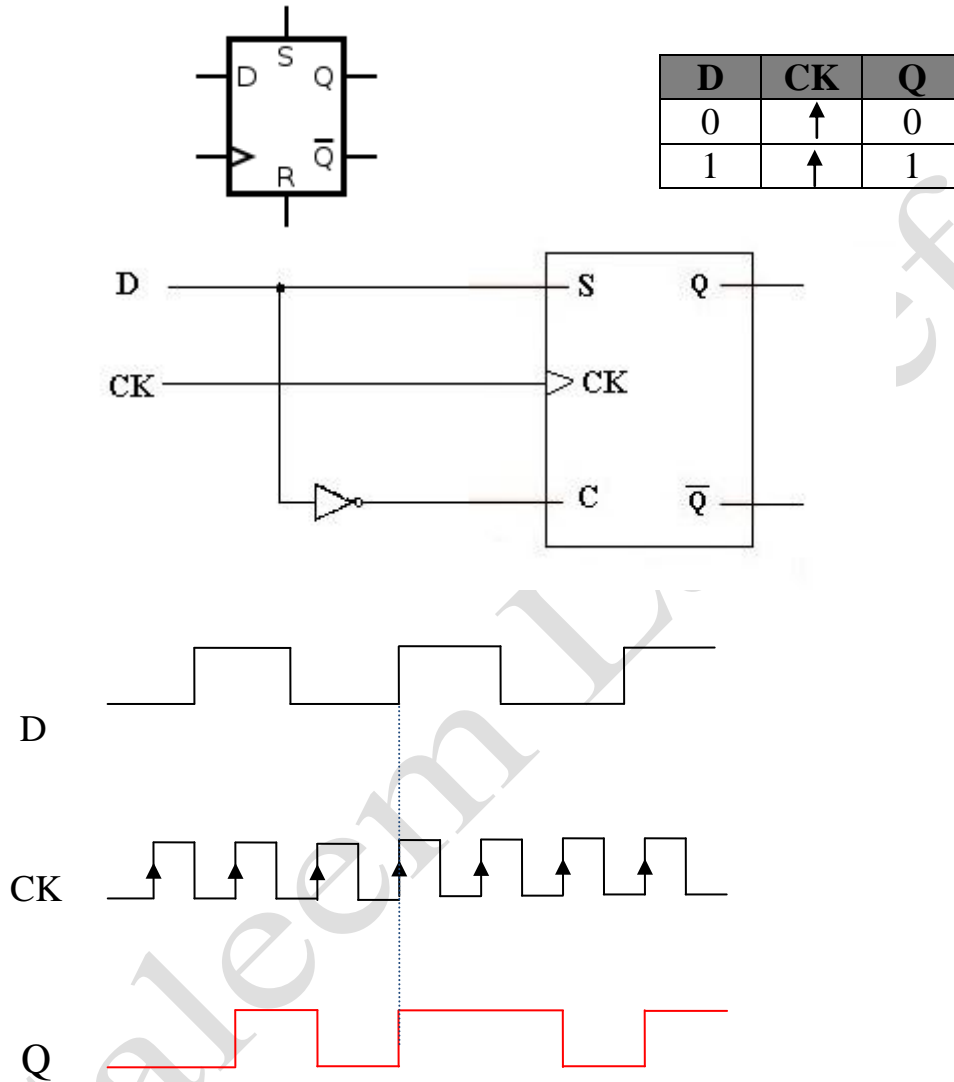
expanding the XOR operator and can be described in a truth table:

Characteristic table				Excitation table			
T	Q	Q _{next}	comment	Q	Q _{next}	T	comment
0	0	0	Hold state (no CLK)	0	0	0	No change
0	1	1	Hold state (no CLK)	1	1	0	No change
1	0	1	Toggle	0	1	1	Complement
1	1	0	Toggle	1	0	1	complement

When T is held high, the toggle flip-flop divides the clock frequency by two; that is, if clock frequency is 4 MHz, the output frequency obtained from the flip-flop will be 2 MHz.

D (Delay) flip-flop :-

The figure below shows the symbol, truth table and internal circuit of D-FF.



The D flip-flop is the most common flip-flop in use today. It is better known as *delay* flip-flop (as its output Q looks like a delay of input D) or *data latch*.

The Q output takes on the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low). It is called the **D** flip-flop for this reason, since the output takes the value of the **D** input or *Data* input, and *Delays* it by maximum one clock count.