Machine cycle

- Time taken by the microprocessor to perform single operation is a machine cycle.
- Each machine cycle is divided into T-states (Clock cycles).
- Time taken to perform on instruction is an instruction cycle, consisting one or more machine cycle.
- Number of T-states makes a machine cycle and a machine cycles makes an instruction cycle.

Machine cycles of 8085

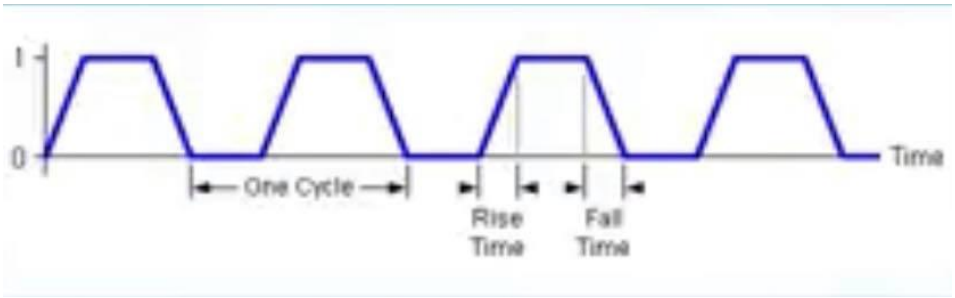
1. Opcode fetch
2. Memory read
3. Memory write
4. I/O read
5. I/O write
6. Interrupt acknowledgment
7. Halt
8. Hold
9. Reset

Instruction cycle

- Time taken by the processor to complete one instruction.
- Consists of one or more than one machine cycle.
- Every instruction has two parts: opcode and operand.
- Instructions are 1 byte, 2 byte and 3 byte long in 8085.
- First machine cycle of every instruction cycle is always opcode fetch i.e. reading op-code.

Timing diagram

- Graphical representation of execution time taken by the processor for any instruction.
- Represents specific instruction cycle in term of machine cycles and T-states.
- 1 T-state represents the operation carried out in one clock period.



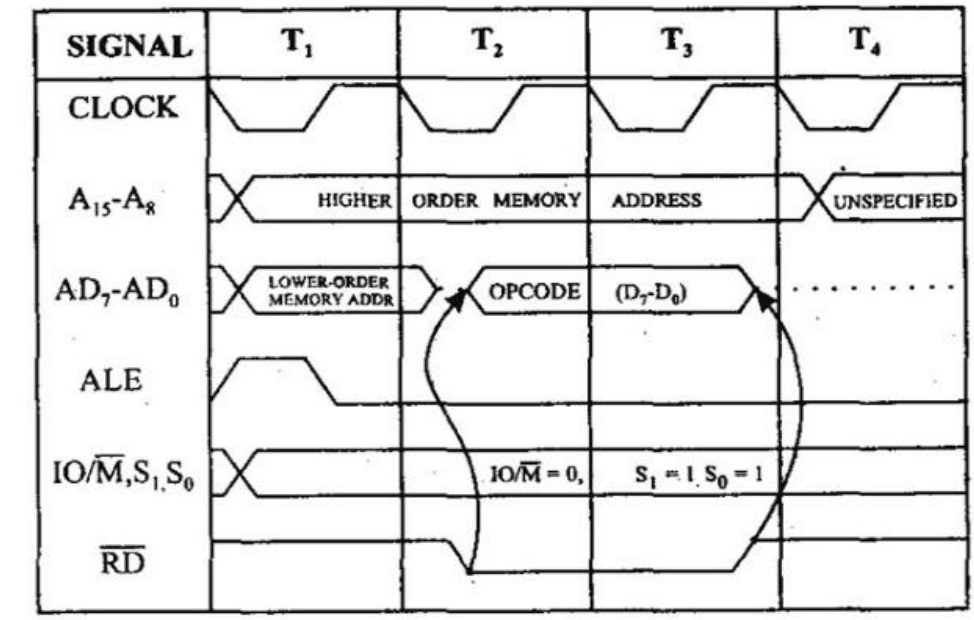
Information for timing diagram

- Timing diagram is drawn for specific instruction, written at a specific location
  e.g. 2000H MOV A,B 78H
- We need to know following values to draw timing diagram:
- Address, where the instruction is written
  e.g. 2000H : A8-A15=20H, A0-A7=00H
- Opcode of the instruction
  e.g. MOV A,B code is 78H, D0-D7=78H
- No. of machine cycles required.(in this case: 1 machine cycle)
- Total no. of T-states (adding T-states of all machine cycles):(4 T-states)

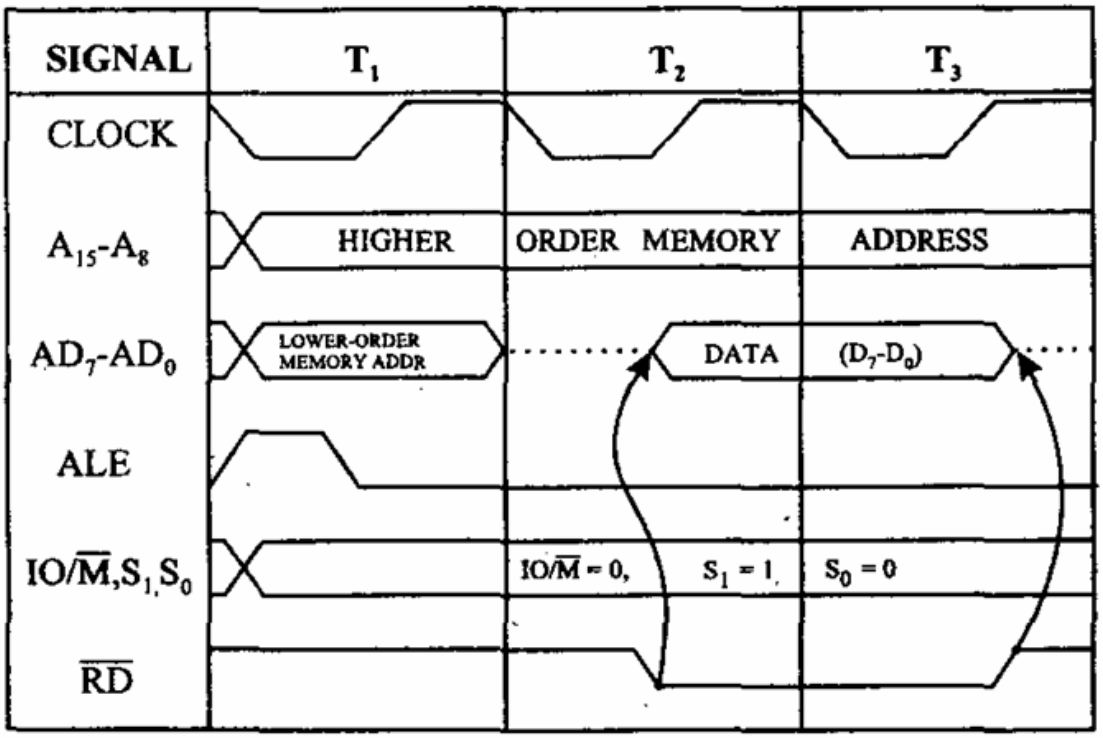
Steps to draw timing diagram

- Make the T-states column wise.
- Draw clock cycles equal to T-states and mark machine cycles.
- Draw higher order address bus (A8-A15) and mark its contents. (20H)
- Draw ALE: it goes high for first clock cycle of every machine cycle.
- Draw low order of multiplexed address/data bus (AD0-AD7). Mark lower order address (00H) wherever ALE is high and mark the data (78H) for next two clock cycles.
- IO/M', RD', WR', S0, S1 values are drawn as per the machine cycle.

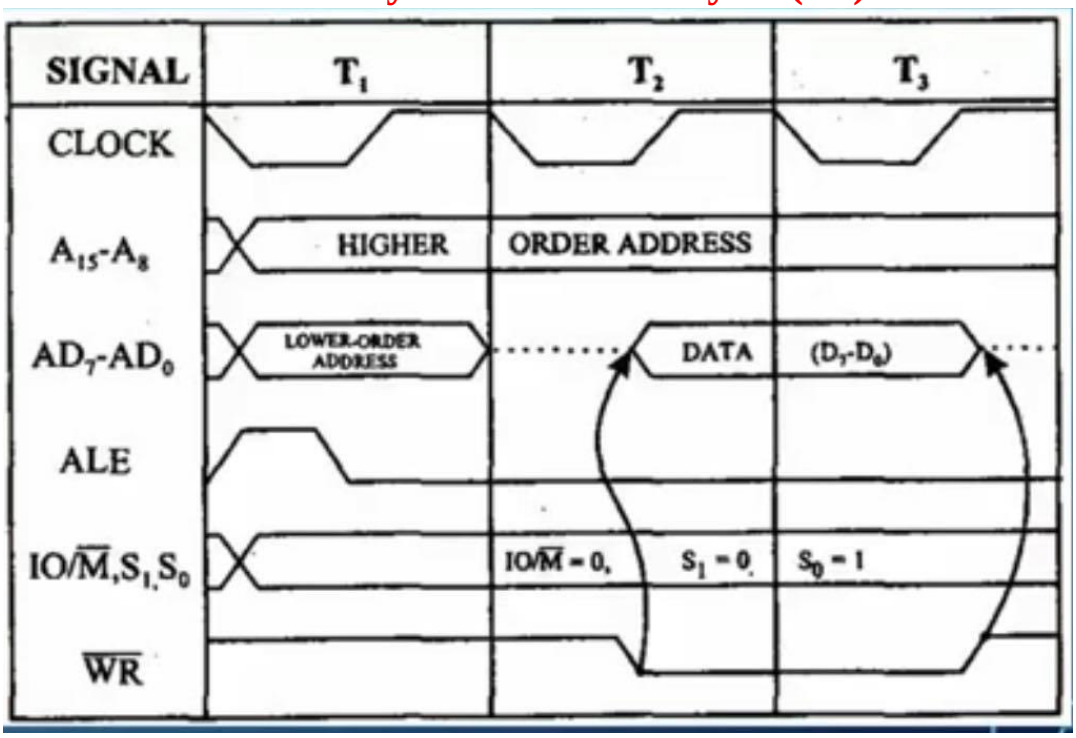
1.Opcode fetch cycle(4T or 6T)



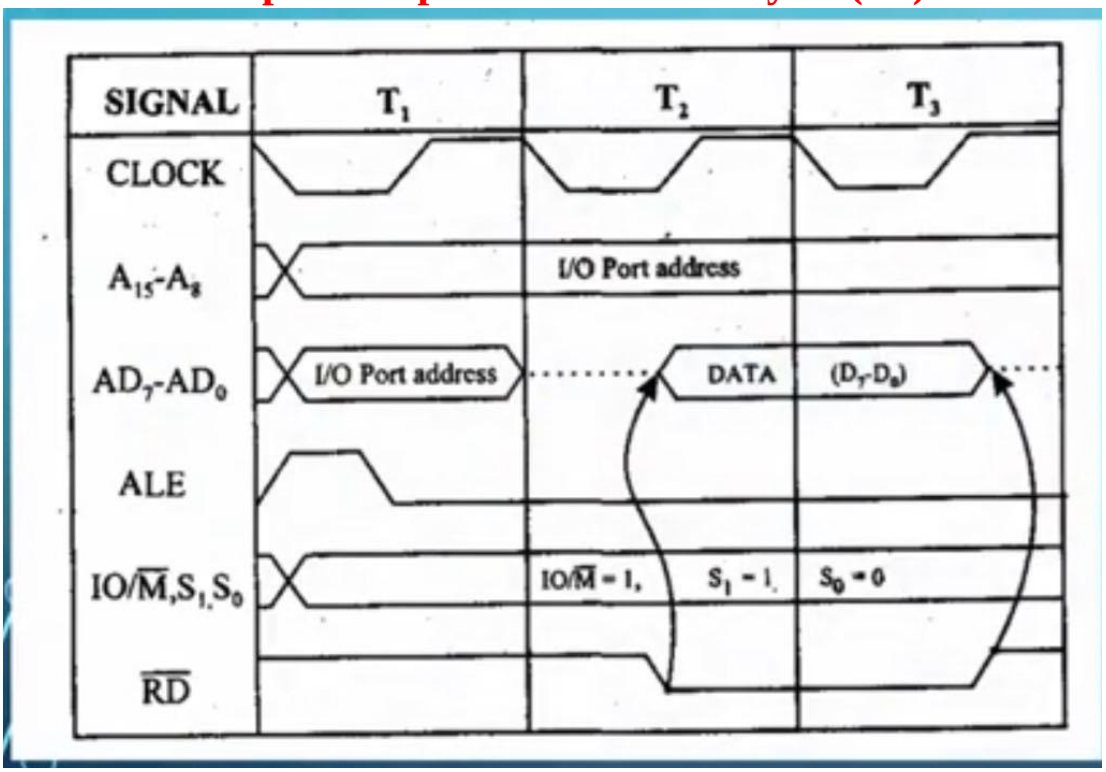
2. Memory read machine cycle (3T)



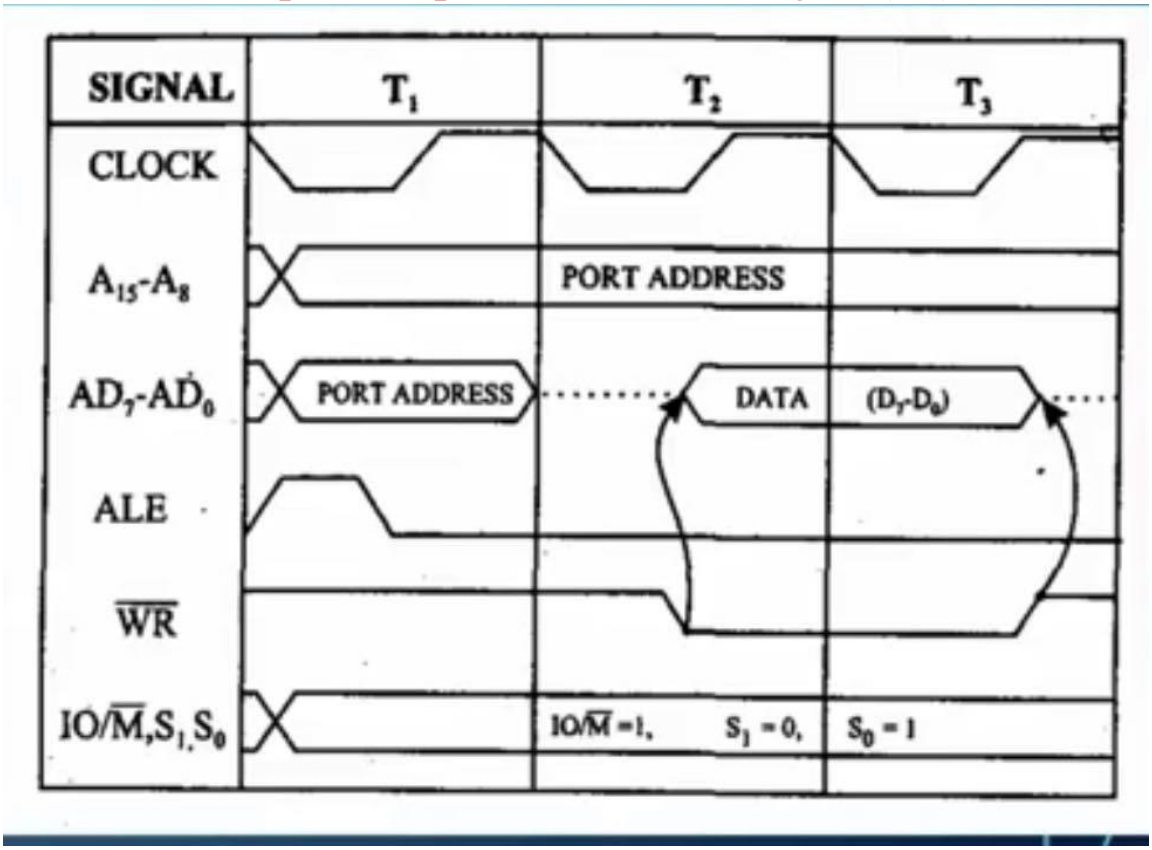
3. Memory write machine cycle (3T)



4. Input/ Output read machine cycle (3T)



5. Input/ Output write machine cycle (3T)



- Timing diagram are graphical representation of the timing details of a processor.
- Each instruction consists of one or more machine cycles, each machine cycle requires more than one T-state to perform the task.
- First machine cycle of any instruction cycle is opcode fetch.
- Timing diagram contains the status of address lines, data lines, control and status signals like RD'. WR', IO/M', S0. S1, ALE.
- ALE goes high for the first clock cycle of every machine cycle.
- When ALE goes high, AD0-AD7 contains address otherwise data.